GX5290 SERIES

MARVIN TEST SOLUTIONS

DYNAMICALLY CONTROLLED HIGH SPEED DIGITAL I/O PXI CARD

- 32 input / output channels, dynamically configurable on a per channel basis
- 256 MB of on-board vector memory
- Supports TTL, LVTTL & LVDS interfaces
- Supports vector rates to 200 MHz
- Operates as a stand-alone card or with up to seven additional synchronous slave boards

DESCRIPTION

The GX5290 Series are a high performance, cost-effective 3U PXI dynamic digital I/O boards offering 32 digital input or output channels with dynamic direction control. The GX5290 Series also supports deep pattern memory by offering 256 MB of on-board vector memory with dynamic per pin direction control and with test rates up to 200 MHz. The single board design supports both master and slave functionality without the use of add-on modules.

FEATURES

The GX5290 Series supports selectable I/O levels of 1.5 V, 1.8 V, 2.5 V, or 3.3 V (TTL, LVTTL, CMOS, LVCMOS). In addition, the GX5290 Series support 32 differential channels for LVDS, M-LVDS, or LVDM logic families. The TTL / LVTTL interface utilizes a programmable voltage source, which sets the output logic levels from 1.4 V to 3.6 V. Programmable thresholds of 1.5 V, 1.8 V, 2.5 V or 3.3 V (5 V compatible) are supported for input signals. Recommended operating input voltage range is from 0 V to 5.5 V.

A windowing method is utilized for PCI memory accesses, which limits the required PCI memory space for each board to only 16 MB, thus preserving test system resources. A direct mode, for continuous data transfer between the test system controller and the I/O pins of the GX5290 Series are also supported.

The GX5290 Series offers 256 MB of vector memory, with 64 Mb per channel. Programmable I/O width allows trading vector width for vector depth. Under software control, the GX5290 Series's vector memory can be configured to support channel widths of 32, 16, 8, 4, 2 and 1 with corresponding vector depths of 64 Mb, 128 Mb, 256 Mb, 512 Mb, 1024 Mb, and 2048 Mb.

The GX5290 Series provides programmable TTL / LVTTL output clocks and strobes, and supports external clock and strobe. A programmable PLL (phase locked loop) provides configurable clock frequencies and delays. An LVDS output clock is also provided.

The GX5290 Series's sequencer can halt or pause on a defined address or loop through the entire memory as well as loop on a defined address range or through a defined block of memory.

PROGRAMMING AND SOFTWARE

The board is supplied with GTDIO/DIOEasy, a software package that includes vector editing, a virtual instrument panel, and 32/64-bit DLL driver libraries and documentation. The virtual panel can be used to interactively program and control the instrument from a window that displays the instrument's current settings and status. In addition, interface files are provided to support access to programming tools and languages such as ATEasy, LabView, C/C++, Microsoft Visual Basic®, Delphi, and Pascal. On-Line help file and PDF User's Guide provides documentation that includes instructions for installing, using and programming the board.

APPLICATIONS

- Automatic Test Equipment (ATE)
- Semiconductor test
- Displays, printers, and disk drive testing
- ASIC testing
- A/D and D/A testing
- Video acquisition / playback applications
- High speed, bi-directional bus testing / emulation

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SPECIFICATIONS
GX5291

INPUT / OUTPUT CHANNEL FEATURES	
Data Direction Control	Dynamically controlled on a per vector and per channel basis
Channels Per Board	32
Channel Configuration Per Board (Software Controlled)	32 / 16 / 8 / 4 / 2 / 1
Maximum Number Channels per Domain	32
Logic Families	TTL/LVTTL/CMOS/LVCMOS (1.5 V, 1.8 V, 2.5 V, 3.3 V, or 5 V compatible)
I/O Levels	TTL/LVTTL/CMOS/LVCMOS: Programmable Output Voltage Level 1.4 V (Min); 3.6 V (Max) Input Threshold (selectable) 1.5 V, 1.8V, 2.5V, or 3.3 V (5V tolerant) Supports standard logic levels Recommended Operating Conditions 0V (Min); 5.5V (Max)
Memory Depth Per Channel	32 Mb - 1Gb, programmable
Channel Timing Skew	± 1 nS
TIMING	
Internal Test Clock (PLL)	
Frequency Range	5 Hz (Min.); 100 MHz (Max.), GX5291-100 50 MHz (Max.), GX5291-50
Accuracy	Greater of (±1Hz or ±0.02% of programmed value) + accuracy of reference clock (PXI 10 MHz or external reference clock)
Jitter	±20 mUI of internal clock frequency, max
Reference	PXI 10 MHz clock or XClk (external clock) input
Internal B Clock Output (TTL / LVTTL)	
Frequency Range	300 KHz (Min.); 100 MHz (Max.), GX5291-100 50 MHz (Max), GX5291-50
Accuracy	Greater of (±1 Hz or ±0.5% of programmed value) + accuracy of the reference clock
Internal Strobe (OSTB) and Output Clock (OCLK) Outputs, Clock and Data Timing	
Logic Levels	TTL / LVTTL / CMOS / LVCMOS, programmable output voltage level, 1.4 V (min) to 3.6 V (max)
Frequency	Internal clock or External strobe, External clock inputs
Programmable Delays (Using Internal Clock Source Only) For Internal Strobe and Output Clock Signals	0 – 27nS in 250pS steps (5 Hz to 100 MHz), GX5291-100 0 – 27nS in 250pS steps (5 Hz to 50 MHz),, GX5292-50
Output Clock to Data Output Delay	__nS, active OCLK clock edge to valid data
Strobe Clock to Data Input	__nS data setup time (min) __nS data hold time (min) Relative to OSTB clock edge
External Test Clock Input	
Frequency Range (Configured as Sample Clock)	0 Hz (Min.); 100 MHz (Max.), GX5291-100 0 Hz (Min.); 50 MHz (Max.),, GX5291-50
Frequency Range (Configured as Reference Clock to PLL)	8MHz to 10.5 MHz
Pulse Width	40% min, 60% max
Input Logic Levels	User selectable I/O level, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, (5 V tolerant), TTL, / LVTTL / CMOS, / LVCMOS
External Strobe Clock Input	
Frequency Range	0 to 100MHz , GX5291-100 0 to 50 MHz, GX5291-50
Logic Levels	TTL / LVTTL / CMOS / LVCMOS Input threshold: 1.5 V, 1.8 V, 2.5 V, or 3.3 V (5 V tolerant)
External Status & Control Signals	
Logic Levels	TTL/LVTTL/CMOS/LVCMOS: Prog. Output Voltage Level: 1.4 V (Min); 3.6 V (Max) Input Threshold: 1.5 V, 1.8 V, 2.5 V, or 3.3 V (5 V tolerant)
Trigger Source	Software, PXI trigger bus, External event, External trigger input (overrides Run command)
External Clock Enable	Internal (software) or External input (via J3 connector)
External Strobe Enable	Internal (software) or External input (via J3 connector)

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External Event Bus	16 input lines with mask and logic AND conditioning
Pause	External pause input overrides Pause command
Pause Latency	10 clock cycles to acquire data after pause deasserts
Run	Run status indicator (J3 connector)
POWER	
3.3 V_{DC}	200 mA (min); 4 A (max)
5 V_{DC}	50 mA (min); 2 A (max)
12 V_{DC}	0.03 mA (min); 0.1 mA (max)
FRONT PANEL CONNECTORS	
J1	I/O TTL Signals, 68-pin VHD connector
J3	Timing/Status Signals, 68-pin VHD connector
J4	Control Signals, 68-pin VHD connector
ENVIRONMENTAL	
Operating Temperature	0 °C to 50 °C
Storage Temperature	-20 °C to 70 °C
Size	3U PXI
Weight	200 g

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INPUT / OUTPUT CHANNEL FEATURES	
Logic Families	TTL/LVTTL/CMOS/LVCMOS (1.5 V, 1.8 V, 2.5 V, 3.3 V, or 5 V), LVDS/LVDM/M-LVDS
I/O Levels	TTL/LVTTL/CMOS/LVCMOS: Programmable Output Voltage Level 1.4 V (Min); 3.6 V (Max) Input Threshold 1.5 V, 1.8V, 2.5V, or 3.3 V (5V tolerant) Recommended Operating Conditions 0 V (Min); 5.5 V (Max) LVDS/LVDM/M-LVDS: Recommended Operating Conditions Voltage Output: -1.4 V (Min.); 3.8 V (Max.) Voltage Input: .05 V (Min.); 3.3 V (Max.)
Memory Depth Per Channel	64 MB - 2 GB
Number of Channels	32 I/O, direction and configuration is dynamically configurable on a per vector and per channel basis
Maximum Number Channels per Domain	256
Channel Timing Skew	1 ns same card, 1 ns between cards
TEST MODES	
Stimulus / Response	Drive / capture data, up to 64 Mb per channel
Real-Time Compare	Drive / compare data against expected data pattern Expect & mask data on a per cycle basis
Real Time Compare Record Memory	1024 x 64 bits of record memory Records compared data and address
Real Time Compare Stop Modes	Stop on defined count errors (max is 1024) Stop when detected failures equal the defined number of failures Stop on defined comparison data value Stop on defined program counter value
TIMING	
Internal Test Clock (PLL)	
Frequency Range	5 Hz (Min.); 100 MHz (Max.)
Accuracy	Greater of (±1Hz or ±0.02% of programmed value) + accuracy of reference clock (PXI 10 MHz or external reference clock)
Jitter	±20 mUI of internal clock frequency, max
Reference	PXI 10 MHz clock or XClk (external clock) input
Internal B Clock Output (TTL / LVTTL)	
Frequency Range	300 KHz (min); 100 MHz (max)
Accuracy	Greater of (±1 Hz or ±0.5% of programmed value) + accuracy of the reference clock
Internal C Clock Output (LVDS/LVDM/MOLVDS)	
Frequency Range	300KHz (min); 100 MHz (max)
Accuracy	Greater of (±1 Hz or ±0.5% of programmed value) + accuracy of reference clock
External Test Clock Input	
Frequency Range (Configured as Sample Clock)	0 Hz (min); 100 MHz (max)

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Frequency Range (Configured as Input to PLL)	8MHz (min) to 10.5 MHz (max)
Pulse Width	40% min, 60% max
Input Level	User selectable I/O level: 1.5 V, 1.8 V, 2.5 V, or 3.3 V (5 V tolerant)
External Strobe Clock Input	
Frequency Range	0 Hz (min); 100 MHz (max)
Logic Levels	TTL/LVTTL/CMOS/LVCMOS: Prog. Output Voltage Level: 1.4 V (Min); 3.6 V (Max) Input Threshold: 1.5 V, 1.8V, 2.5V, or 3.3 V (5V tolerant)
External Status & Control Signals	
Logic Levels	TTL/LVTTL/CMOS/LVCMOS: Prog. Output Voltage Level: 1.4 V (Min); 3.6 V (Max) Input Threshold: 1.5 V, 1.8 V, 2.5 V, or 3.3 V (5 V tolerant)
Trigger Source	Software, PXI trigger bus, External event, External trigger input (overrides Run command)
External Clock Enable	Internal (software) or External input (via J3 connector)
External Strobe Enable	Internal (software) or External input (via J3 connector)
External Event Bus	16 input lines with mask and logic AND conditioning
Pause	External pause input overrides Pause command
Pause Latency	10 clock cycles to acquire data after pause deasserts
Run	Run status indicator (J3 connector)
POWER	
3.3 V_{DC}	200 mA (min); 4 A (max)
5 V_{DC}	50 mA (min); 2 A (max)
12 V_{DC}	0.03 mA (min); 0.1 mA (max)
FRONT PANEL CONNECTORS	
J1	I/O TTL Signals, 68-pin VHD connector
J2	I/O LVDS Signals, 68-pin VHD connector
J3	Timing Signals, 68-pin VHD connector
J4	Control Connector, 68-pin VHD connector
ENVIRONMENTAL	
Operating Temperature	0 °C to 70 °C
Storage Temperature	-20 °C to 70 °C
Size	3U PXI
Weight	200 g

GX5293

INPUT / OUTPUT CHANNEL FEATURES	
Logic Families	LVTTL/CMOS/LVCMOS (1.5 V, 1.8 V, 2.5 V, or 3.3 V) , LVDS/LVDM/M-LVDS
I/O Levels	LVTTL/CMOS/LVCMOS: Programmable Output Voltage Level 1.4 V (Min); 3.6 V (Max) Input Threshold 1.5 V, 1.8V, 2.5V, or 3.3 V Recommended Operating Conditions 0V (Min); 3.6V (Max) LVDS/LVDM/M-LVDS: Recommended Operating Conditions Voltage Output: -1.4V (Min.); 3.8 V (Max.) Voltage Input: .05V (Min.); 3.3V (Max.)
Memory Depth Per Channel	128 MB
Number of Channels	16 I/O, direction and configuration is dynamically configurable on a per vector and per channel basis 32 I/O, for vector rates <100 MHz
Maximum Number Channels per Domain	256
TIMING	
Internal Test Clock	
Frequency Range	5 Hz (min); 200 MHz (max)
Resolution	Greater of 1 Hz or .5%
Internal B Clock Output (TTL / LVTTL)	
Frequency Range	300 KHz (min); 200 MHz (max)
Resolution	Greater of 1 Hz or .5%
Internal C Clock Output (LVDS/LVDM/MOLVDS)	
Frequency Range	300KHz (min); 200 MHz (max)
Resolution	Greater of 1 Hz or .5%
External Clock Input	
Direct	0 Hz (min); 200 MHz (max)

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PLL	3 MHz (min) 200 MHz (max)
Pulse Width	40% min, 60% max
Input Level	User selectable I/O level: 1.5 V, 1.8 V, 2.5 V, or 3.3 V
POWER	
3.3 V_{DC}	200 mA (min); 4 A (max)
5 V_{DC}	50 mA (min); 2 A (max)
12 V_{DC}	0.03 mA (min); 0.1 mA (max)
ENVIRONMENTAL	
Operating Temperature	0 °C to 50 °C
Storage Temperature	-20 °C to 70 °C
Size	3U PXI
Weight	200 g

Note: Specifications are subject to change without notice

ORDERING INFORMATION

GX5291-50	Dynamic Digital I/O (3U), 32 ch. up to 50 MHz w/128MB On-Board Memory, 32-ch Domain
GX5291-100	Dynamic Digital I/O (3U), 32 ch. up to 100 MHz w/128MB On-Board Memory, 32-ch Domain
GX5292	Dynamic Digital I/O (3U), 32 ch., per Pin Control, up to 100 MHz w/256MB Memory & LVDS
GX5293	Dynamic Digital I/O (3U), 16 ch., per Pin Control, up to 200 MHz w/256MB Memory & LVDS
SOFTWARE	
DIOEasy	Digital I/O Vector Development Software
DIOEasy-FIT	DIOEasy file import tool kit converts STIL, WGL, VCD/EVCD files to Marvin Test Solutions digital file formats for the GX529x and GX5055 digital I/O cards
DIOEasy-FIT-UG	Upgrade for DIOEasy file import tool kit
DIOEasy-FIT-S1Y	Renew DIOEasy-FIT Subscription and Support (1 Year)
DIOEasy-FIT-S2Y	Renew DIOEasy-FIT Subscription and Support (2 Years)
DIOEasy-FIT-S3Y	Renew DIOEasy-FIT Subscription and Support (3 Years)
DIOEasy-FIT-EXP6	Renew Expired DIOEasy-FIT Subscription and Support (expired 1 day to 6 months)
DIOEasy-FIT-EXP24	Renew Expired DIOEasy-FIT Subscription and Support (expired 7 to 24 months)
DIOEasy-FIT-SUP	1-year Support only for DIOEasy-FIT (no upgrades)
DIOEasy-DS	2 days DIOEasy training at Marvin Test Solutions (Irvine, CA) for 1-3 persons. Call for larger groups.
DIOEasy-DS2	On-site, 2-days DIOEasy training seminars for 1-3 persons. Call for larger groups.
ACCESSORY	
TS-900e-5G-BMC	Blind mate connectors (one pair), DC - 40 GHz, 2.92mm
GT95015	Connector Interface for all 5xxx/35xx, SCSI to 100 Mil Grid, Differential
GT95021	2 ft. Shielded Cable for all 5xxx/35xx (68 Pin)
GT95022	3 ft Shielded Cable for all 5xxx/35xx (68 Pin)
GT95022E	3 ft Shielded Cable for all 5xxx/35xx (68 Pin) Not Terminated One End
GT95025	Connector Interface, 68-Pin SCSI to TTI Testron 170-Pin Signal Block
GT95028	10 ft shielded cable for 5xxx/35xx products (68 Pin)
GT95031	6 ft Shielded Cable for all 5xxx/35xx (68 Pin)
GT95035E-48	Shielded Flying Lead Cable for all 5xxx/35xx (68 Pin), 48".
GX98303	3U "Wireless" Scout Adapter for GX528x/GX529x/GX564x/GX5733 (200-Pin Connector)

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